AMS-2 DAQ SYSTEM
J-Crate
HARDWARE DESIGN REQUIREMENTS

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AMS-2 DAQ SYSTEM J-CRATE HARDWARE DESIGN REQUIRNMENTS

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07	Added cold state operations profile diagram. Updated to new STS 1553 configuration. Documented PRST handling for boot commands.	20 Dec 2002	PAD
07b	Added HRDL test requirements	18-Jul-03	PAD

CONTENT

TABLE OF FIGURES

1 The AMS-02 Data Acquisition System (DAQ)

This document provides information about the system design of the J-Crate. To support the understanding of the system this introduction discusses the AMS Data Acquisition System (DAQ) from the bottom up.

1.1 The DAQ Parts

As shown in Figure 1-1, the main DAQ elements are arranged in a tree structure with:
Front-End DAQ Modules as the lowest level, which include a "Common Digital Part" (CDP). This front end provides digitization and data compression/reduction for the detector's sensors.
A two level hardware trigger mechanism, based on signals provided by the detectors and their front ends which regulate the data flow within the tree via
Intermediate levels of Command Distributor Data Concentrator (CDDC) nodes. These are used to buffer and concentrate data obtained from the detector front ends and distribute commands from the DAQ master.
The AMS-Wire signaling system used to transport data among the DAQ system components (CDP<>CDDC<>CDDC<>JMDC).
The Main DAQ Computers (JMDCs) which serve both as the top level of the data collection tree or DAQ Master (or Event Builder) and as the bridge to the International Space Station (ISS) High Rate Date Link (HRDL) system (and the RS422 interface to the Shuttle) via the High rate Interface module (JHIF).
In the current design, two CDP's are physically located on an xDR2 Board, where x=T, U, S, R or E corresponding to the Tracker, TRD, Scintillator (ToF+ACC), RICH or ECal detectors. These boards also interact with trigger and timing signals. The lowest level CDDCs are located in the same crate as a set of xDR's on JINF boards, which also distribute trigger and timing signals. The next level of CDDC's are centrally located on JINJ boards.

1.2 Purpose of the DAQ System

- Provide an orderly detection of events.
- Prepare a digital representation of the event data within each detector.
- Introduce minimal extra dead time (as close to zero as possible) on top of what is defined by the Tracker readout time (83 us).
- Provide preliminary detector dependent processing, including reduction (compression).
- Gather the event parts (segments) from the detectors via the CDDC tree.
- Assemble these event parts into a coherent event.
- Suppress events that are not of interest.
- Organize the transport of the events and retrieved values to the ground for study.
- Provide a commanding mechanism including setting parameters and states.
- Provide a retrieval mechanism for values of parameters, states, and observations.

1.3 Block Diagram of DAQ

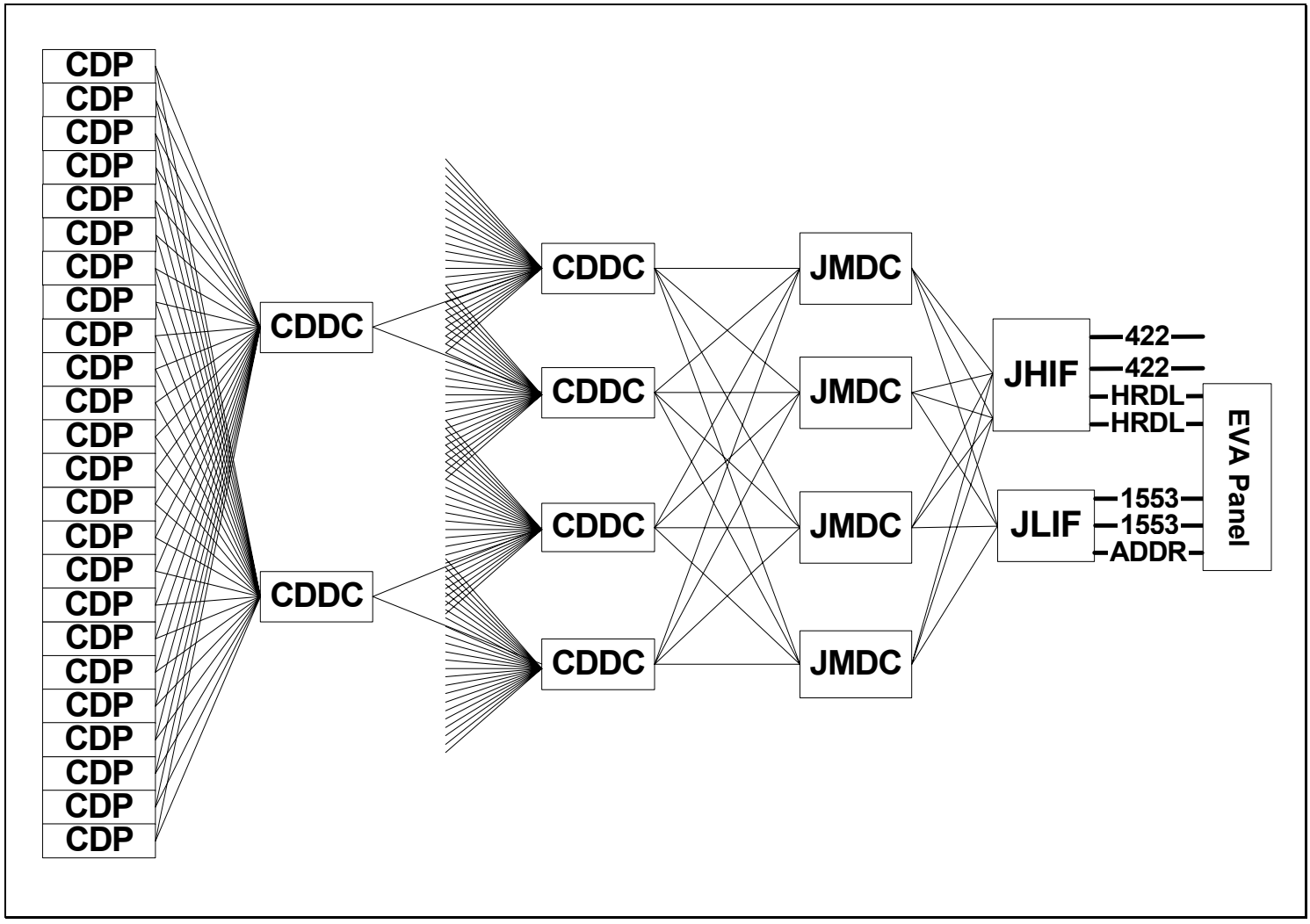


Figure 1-1 - The DAQ Tree

Note: Many CDPs and CDDCs on the left side of the diagram are omitted for clarity. The connections to CDDC boxes are all AMSWire. The connections between the JMDC and JHIF/JLIF carry other types of serial data streams.

1.4 Front-End DAQ Module

Each AMS detector has unique preliminary signal condition circuits consisting, typically, of various ASIC amplifiers/shapers, analog multiplexers, and A/D converters. The conditioned signals for a detector are fed into its' Front-end DAQ module. While each detector presents unique challenges in organizing its analog and digital data, they all share some common architecture within their Front-end DAQ modules. The common portion is called the Common Digital Part (CDP). It is important to note that while the circuitry will share a common architecture among detectors, the gate array logic and firmware are not in common.

The CDP provides detector unique data processing, a buffer area to store several fixed sized buffers of event data, and a firmware based AMS-Wire interface connected to the lowest level of the CDDC tree.

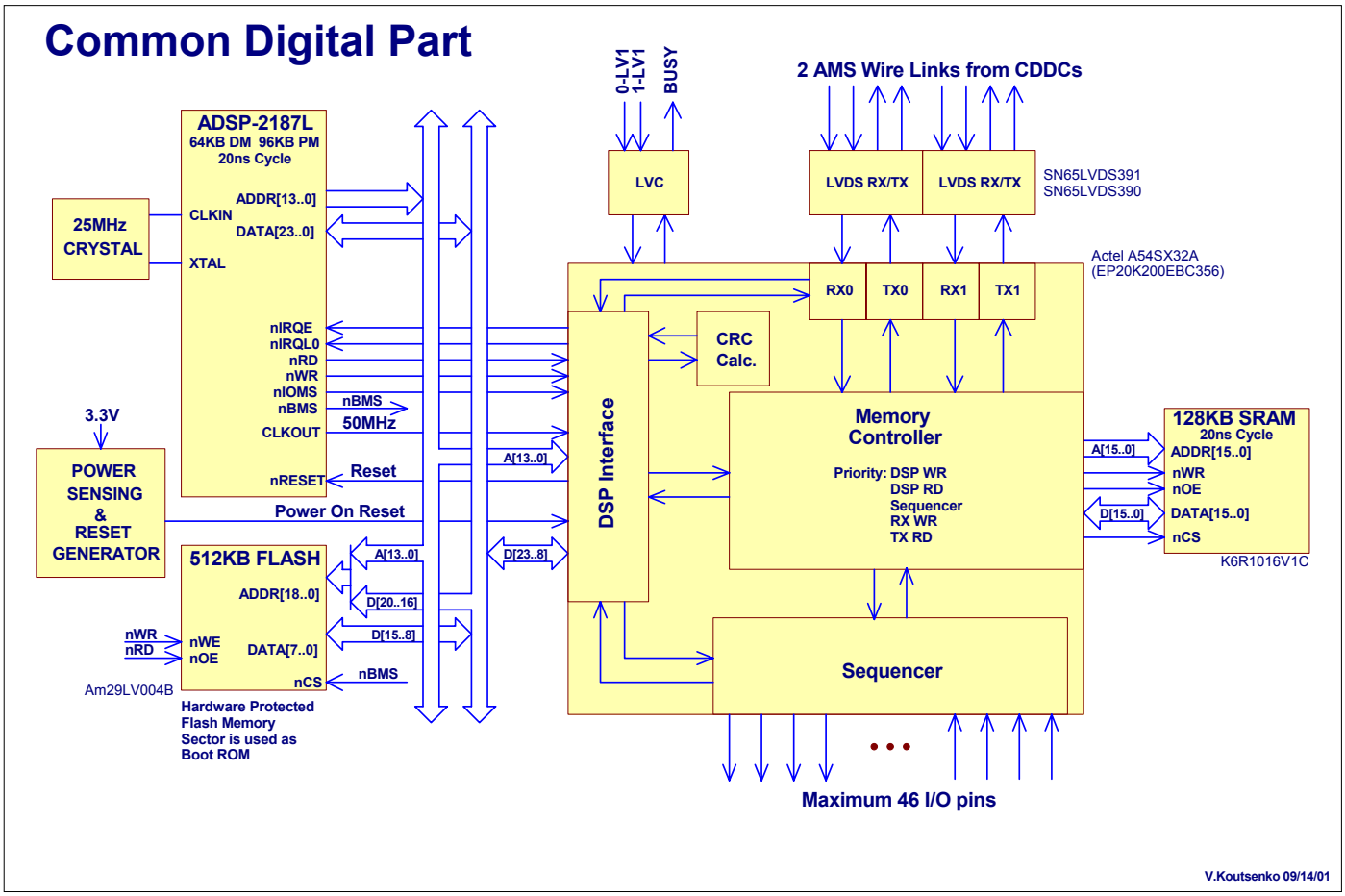


Figure 1-2 - Common Digital Part

A CDP block diagram is presented in Figure 1-2. The basic functions of the Common Digital Part are the following: record digitized raw events; process them in order to reduce the size without losing physics information; and respond to commands from the master CDDC. Buffering of raw events in the CDP is provided in order to smooth the event timing fluctuations.

1.5 Data Flow, Level-1 Trigger and BUSY.

The flow of data within the DAQ Tree is regulated by the trigger and timing system using the Level-1 trigger (LV1) and BUSY signals.

The Level-1 trigger signal indicates that a particle of interest may have passed though the experiment. It is based on signals from the ToF, ACC and ECal detectors which are continuously monitored. When any of a series of predetermined configurations of these signals are observed the LV1 signal is generated and distributed (unless the system is BUSY, see below) to all the Front End DAQ modules and, after appropriate delays for signal shaping, they commence to digitize and buffer their associated detector signals. This is referred to as an “event”, and the set of digitized data collected in response to a particular trigger as the “raw event data”. In the current design of AMS 02 it totals to about 0.6 MByte.

After the data has been buffered it is processed by the CDP and made available for collection by the upper nodes in the DAQ Tree. This processed data is what is usually

meant by “event data”. The expected size is a few Kbytes.

However, this process of digitization and buffering is not instantaneous and each CDP has a finite buffering capacity (at least four raw events), so at any given instant the CDP may be unable to commence data collection. To ensure that the information for each event is collected from the complete detector a system of BUSY signals is used.

When a detector front end receives the LV1 pulse, it raises its BUSY signal. When the detector front end completes its digitization (and has placed the data into a buffer) a check is made to see if another buffer is available. If a buffer is available the detector front end BUSY is dropped. If all buffers contain raw event data the detector front end keeps its BUSY signal active.

The system BUSY is the logical-or of all of the detector front-end BUSY signals. When the system is busy, that is when any of the detector front ends are asserting a BUSY signal, the trigger logic inhibits the distribution of the LV1 signal.

1.6 Data Volumes and Throttling

It is key to note that the design of this system is such that the data gathering speed is governed by: 1) the rate of physics events, 2) the interval required to digitize the detector signals, 3) the system’s ability to move data to it’s top-level component, the JMDC and 4) the rate and level of filtering and compression in the JMDC. Once data is collected it will not be discarded due to system overloading. If the system becomes congested with data the acquisition of new data is prevented (“throttled”).

The raw data handling requirements of the system are not clearly defined yet. Events nominally will occur about 100 to 2000 events per second dependent on orbital location and solar flare activity. Modeling based on AMS-01 indicates Level-1 triggering will reject an estimated 0 to TBD percent of these events. Events are estimated to be between 1000 and 4000 bytes of data when fully assembled. Nominally events are about 2000 bytes.

Using these estimates the MDC must be capable of handling a raw event data “peak average” of 2000 events per second peak, times 2000 bytes per event average, thus 4 Mbytes/second.

The MDC software provides a filtering mechanism called the Level-3 trigger. This filter examines each event to determine if it is of interest. The Level-3 trigger reduces the event traffic by an estimated TBD percent.

The long-term commitment from NASA is to provide at least 2 Mbits per second of downlink data from AMS-2 on average. The combination of Level-3 filtering and data throttling will need to be tuned to correspond to this limit.

1.7 AMSWire

AMSWire is a communications system consisting of wiring and a signaling protocol. AMSWire’s design is derived from IEEE 1355 and influenced by SpaceWire, an ESA project. The AMSWire system provides a master slave communication environment which supports a signaling rate of 100 Mbits per second and transfers of up to 10Mbytes per second.

1.8 CDDC

Figure 1-3 shows the CDDC organization.

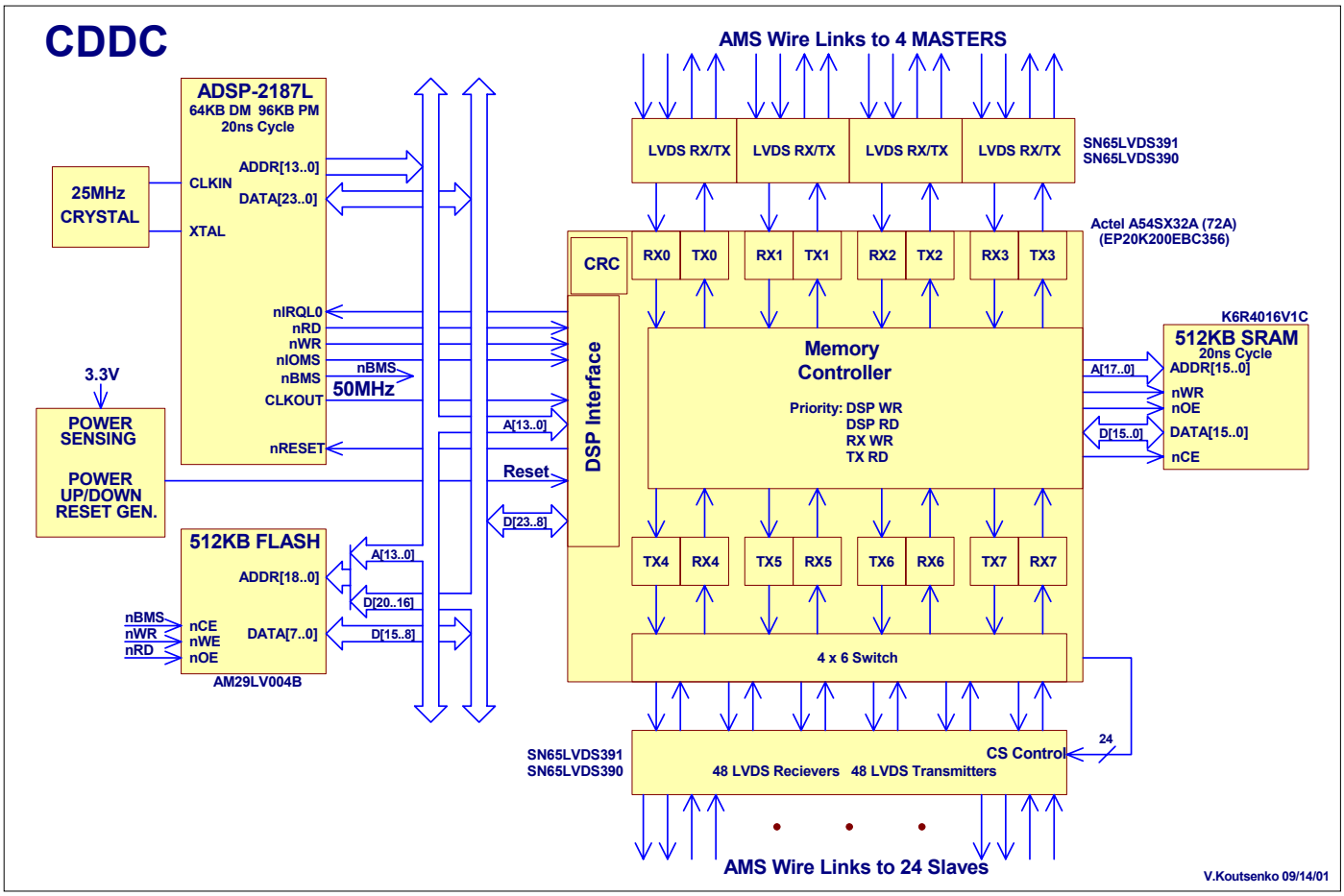


Figure 1-3 - CDDC Block Diagram

By design it is similar to the CDP with the following notable differences: There are 4 instead of 2 links to the masters (though not all may be used in all applications). The front end sequencer is replaced with 4 AMSWire ports which may be multiplexed to 24 seperate links to slaves. The SRAM size is increased to 512KB.

1.9 DAQ Tree

The DAQ tree is used to provide command distribution and the event and other data collection paths via the CDDC nodes. The operational concept should be described somewhere else. The key points are that the CDDC provides two or four (as shown) AMSWire ports and links to receive requests from its master at any time and reply to those requests. It also provides 4 ports, which are multiplexed to up to 24 AMSWire links to place requests with its slaves and receive their replies. This means that up to 8 data paths can be simultaneously active within the CDDC – either transmitting or receiving. In addition, any data processing, for example of the data from its slaves before transmission to a master, is performed within the attached DSP.

1.10 The Main DAQ Computer (MDC)

At the top level of the DAQ tree are four Main DAQ Computers (each a JMDC). There are four for redundancy only. Nominally one of these is selected to be the active DAQ tree head and perform event building. Other JMDCs may be active in the coordinated processing of event data, engaged in other tasks or powered off.

Once this JMDC completes collection of all data associated with an event it assembles this data into a cohesive data structure. The event data structure is encapsulated with an AMS Block. All data flowing within AMS is contained within AMS Block structures.

Within the JMDC, the Level-3 filtering system further validates if the event is of interest or is to be discarded.

Event data selected for collection is placed into the JBU RAM buffer. The JBU buffer is used to accommodate data collection during times when AMS does not have a means to transmit the data down the High Rate Data Link (HRDL) system (assuming ISS operation) or RS422 to the STS KU (for Shuttle operation) and to smooth the flow of data.

1.11 External Interfaces

This section introduces the external interfaces to the J-Crate.

1.11.1 1553 Interface

AMS experiment is connected to the STS and ISS by a 1553 interface. This interface provides a standard NASA command and control interface.

1.11.2 CAN Bus

AMS provides internal command distribution and status gathering via a CAN bus network connecting Universal Slow Control Modules (USCM) and other modules. For redundancy there are two CAN buses interconnecting all of these CAN nodes.

Each MDC has two CAN interfaces, one to each of the CAN busses. These interfaces are active and supported by a microprocessor even in the event the MDC itself is not operational. This allows one MDC to reboot a wayward MDC.

The MDC uses the CAN mechanism to manage the housekeeping data (often called health and status data in the space community) of the entire experiment. A mechanism is provided to incorporate this data into the HRDL stream.

1.11.3 High Rate Data Link (HRDL)

The HRDL system is the fiber optic pathway on the International Space Station (ISS) used to handle an attached payload's science data. The implementation of the HRDL system is done using the TAXI protocol and Teledyne electro-optical components. HRDL is specific to the ISS.

1.11.4 RS422 High Rate Link

In the Space Shuttle, both pre-launch and during the flight to the ISS, AMS-02 will be checked out to assure certain major systems are operating nominally. An RS422 link to the Shuttle aft flight deck provides connectivity to the ground and to an on board laptop system (ACOPjr aka DDRS-2). The crew can change this connection. An additional connection is made in parallel to the STS KU system for telemetry down link. Before launch the connection will be to the T0 cable and hence to the ground. During flight the connections will be to both the KU system (TX only) and ACOPjr (TX and RX).

1.11.5 Alternative Commanding Paths

The MDC supports equal abilities for command and control among the 1553, RS422, and HRDL interfaces. The system is designed to allow any of these interfaces to assume the duties of the primary command and control interface to support operations on the shuttle and on the station, to optimize performance and to minimize single point failures.

2 The J-Crate *(finally!)*

The principal hardware elements of the J-Crate are (see Figure 2-1):

a) Four independent Main DAQ Computers (JMDC) which each contain:
   i) a single board computer (JSBC),
   ii) a memory buffer peripheral board (JBU),
   iii) a set of peripheral modules on 1 to 4 boards (JIMs) which interface to:
      (1) several AMSWire links (JIM-AMSW),
      (2) the AMS-wide slow control dual CAN busses (JIM-CAN),
      (3) two HRDL transceivers (JIM-HRDL),
      (4) an RS422 transceiver (JIM-422),
      (5) two LRDL transceivers for ISS and one for STS (JIM-1553).
   iv) a compact PCI format backplane (32bit, 3.3 and 5 VDC).

b) A High Rate interface board (JHIF), containing:
   i) two HRDL Fiber Optic Transceivers (JFOM),
   ii) an RS422 transceiver (J422).

c) A Low Rate interface board (JLIF) containing
   i) two LRDL transceivers (J1553).

d) A Backplane (JBP) which contains:
   i) the four cPCI backplanes of the four JMDCs (a.iv),
   ii) A two bit JMDC identifier,
   iii) interconnections between the JHIF and JLIF boards and their respective JIMs,
   iv) AMSWire interconnections between the JMDCs via the JIM-AMSW modules,
   v) Power feeds for the JLIF and JHIF.

e) The mechanical crate body to hold the boards and backplane.

Closely associated with the J-Crate is a power supply (JPD) and the interconnections to it. Each of these elements will be discussed in turn.

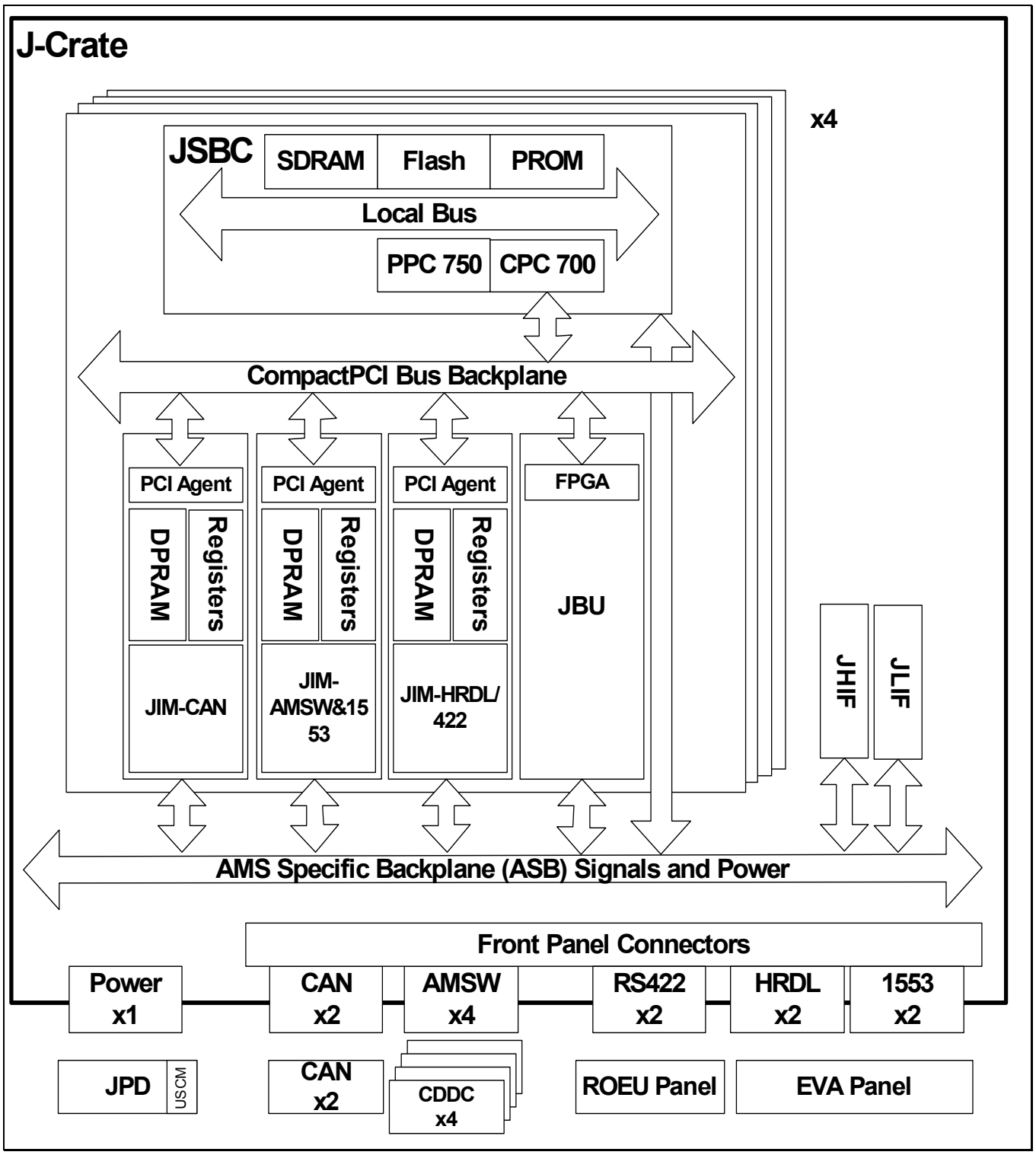


Figure 2-1 - J-Crate, JPD, and Other Connections (USCMs not shown).

2.1 JMDC

Each JMDC consists of the following.

2.1.1 JSBC

A CompactPCI 6U single board computer based on the PowerPC 750 chip set.

2.1.2 JBU

A CompactPCI 6U board providing 2Gbytes of SDRAM buffer storage.

2.1.3 JIM-xxxx

Interface modules housed on CompactPCI 6U boards. Used to communicate with other parts of the system. The JIM-422 and JIM-HRDL modules are combined on the JIM-HRDL/422 PCB and JIM-AMSWIRE and JIM-1553 are combined in the JIM-AMSW&1553 PCB.

The following are the JIM modules.

2.1.4 JIM-422

The JIM-422 interface provides bi-directional buffering (queuing) of character data and conversion to/from serial signaling with a clock. JIM-422 generates/receives RS422 signals that are connected to the J422 module located on the JHIF (J High rate InterFace) board.

In the J422 module the signals are: concentrated/fanned-out, buffered, and routed to the appropriate connectors.

The effect of the JIM-422 board is to provide a single full duplex serial connection for an MDC at RS422 signaling levels. The effect of the J422 interface on the JHIF board is to distribute this signal to two external connections and regenerate this RS422 signal set.

By nature of the design only one of the two external connections will be capable of transmitting data to JIM-422.

2.1.5 JIM-HRDL

The JIM-HRDL interface provides bi-directional buffering (queuing) of character data and conversion to/from TAXI serial signaling. JIM-HRDL generates/receives electrical signals that are connected to the JHIF board.

On the JHIF board the signals are: concentrated/fanned-out, converted to/from light, and routed to the appropriate connectors.

The effect of the JIM-HRDL board is to provide a single full duplex TAXI serial connection for a JMDC. The effect of the JFOM interface on the JHIF board is to distribute and convert this signal to/from a pair of fibers.

2.1.6 JIM-AMSW

The AMSWire interface for JMDC provides intelligent bi-directional buffering and AMSWire connections. Four connections are used to connect to the top level

CDDCs (JINJs) and the remaining are used to interconnect to the other JMDCs.

2.1.7 JIM-CAN

The JIM-CAN interface provides intelligent bi-directional buffering (queuing) and an intelligent interface to the two CAN (Controller Area Network) busses.

2.1.8 JIM-1553

The JIM-1553 interface provides a MIL Standard 1553 command and control bus. The JIM-1553 module provides a transceiverless standard dual redundant 1553 bus interface. The logic state 1553 signals are fanned in/out to the JLIFs two modules which provides the transceiver and isolation transformers. See **Figure 3-5**.

In addition to providing the 1553 functionality this interface provides the support for the CPU to read the 1553 address bits and the JBP_STS bit indicating STS operations.

One or more JIM-1553 modules also have populated an addition 1553 interface with transceivers. This interface is used during Shuttle operations. This interface connects directly to the integration hardware (ROEU panel) and does not operate through the JLIF.

2.2 JHIF

The JHIF board provides the interfaces to the HRDL and RS422 systems. Its functions are detailed below.

2.3 JLIF

The JLIF board provides the interface to the 1553 system and ancillary connections for ISS operations. Its functions are detailed below. See **Figure 3-5**.

2.4 JBP

A backplane providing four CompactPCI backplanes plus accommodations for addition interface boards. The CompactPCI backplanes are adapted for the AMS system. Support is provided for +3.3, +5, and ±5.2-volt power, geographical MDC addressing, and application specific backplane signals.

2.5 JPD

The JPD provides voltage conversion and power management for the J crate. The JPD consists of an assembly of DC-DC converters mounted on 6U VME format boards with an associated Universal Slow Control Monitor (USCM).

3 External Interface Adapters

3.1 JHIF

The JHIF is a CompactPCI form factor board, but with no connection to the cPCI busses. It is not part of the four JMDCs but is housed within the J-Crate and integral to the operation of the high rate communications systems (RS422 and HRDL).

The JHIF board has two types of modules: J422 and JFOM. The J422 module provides interfaces for the serial RS422 data streams and the JFOM modules provide interfaces for the fiber optic based HRDL data streams.

Current planning is for two JFOMs to be implemented along with one J422 on a single JHIF board. Each of these three modules is to be implemented as an electrically isolated circuit.

It is key that there should be no common failure points to these systems and that these modules be as resistant to failure as practical.

3.1.1 Details for HRDL External Interfaces

Figure 3-1 illustrates how the HRDL signals are handled.

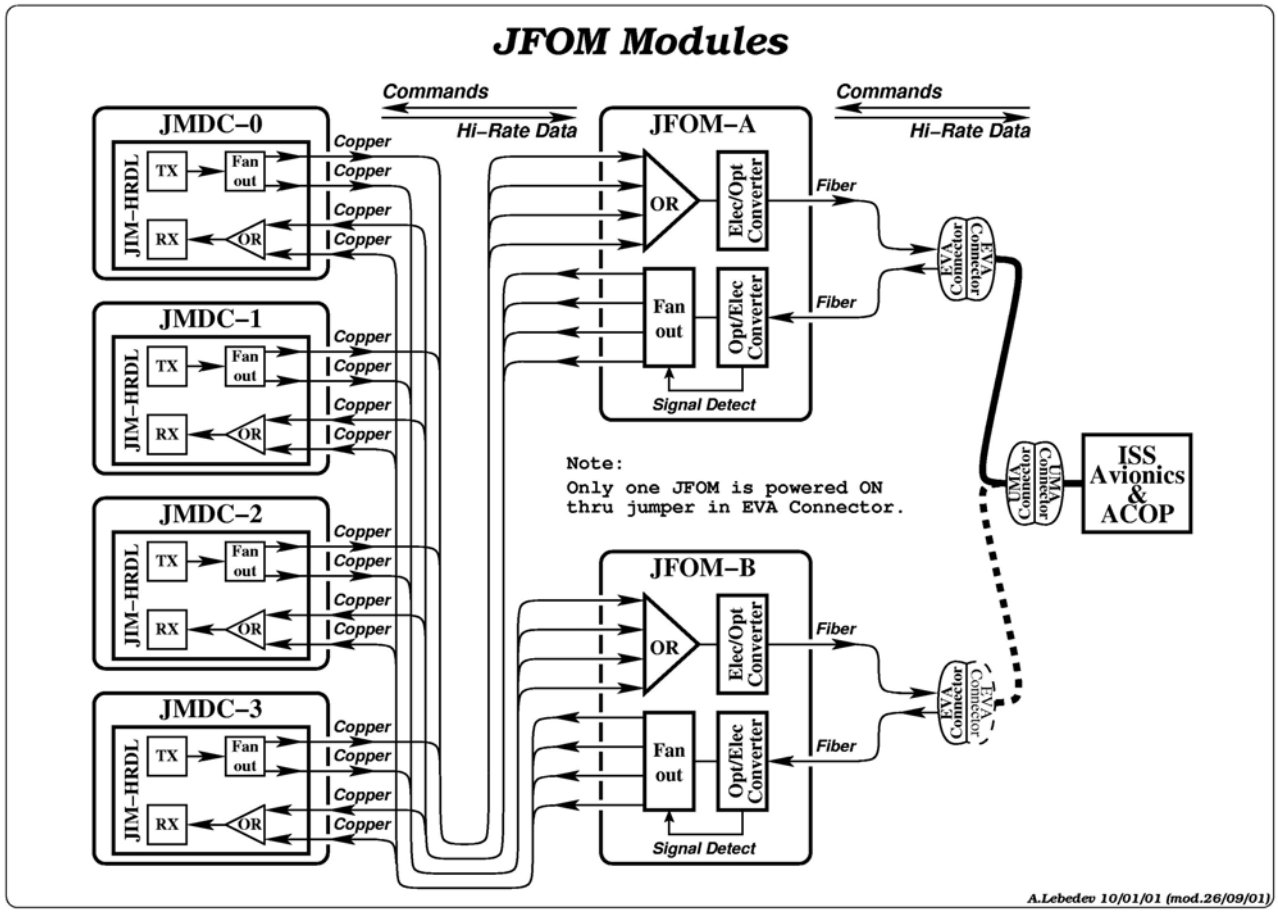


Figure 3-1 – HRDL Integration

3.1.2 JFOM Implementation Details

The JFOM module can receive/transmit serial TAXI signals from/to any of the JIM-HRDLs in each of the four JMDCs. The TAXI signals are concentrated/fanned-out and converted to/from light. The resulting optical signals are connected to the ISS via an EVA connector.

The second JFOM module connects to the second fiber EVA connector.

3.1.3 The J422 Serial Interface

Figure 3-2 illustrates how the J422 signals are handled.

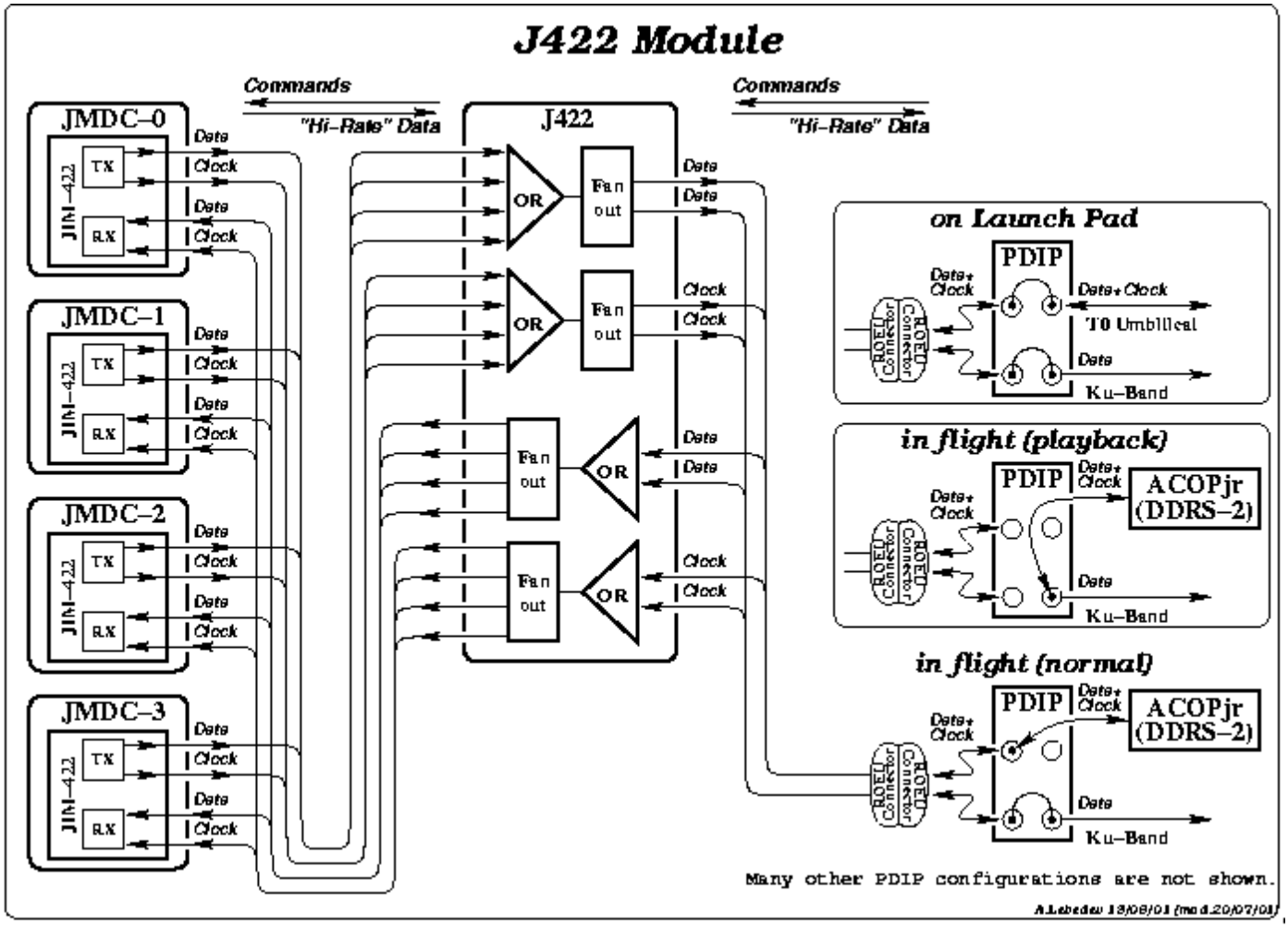


Figure 3-2 – RS422 Integration

3.1.4 J422 Implementation Details

The J422 module receives RS422 electrical signals carrying a full duplex serial data stream with independent clocks from one of the four JIM-422 modules in the four MDCs. These signals are concentrated or fanned-out and re-generated for transmission as RS422 signals on two separate local connections.

The two receive lines will not be active simultaneously.

3.1.5 Power Management on the JHIF Board

The 2 JFOM's located on the JHIF are electrically independent. The power lines (+5.0/-5.2V, RTN) for each are supplied from the backplane. As far as the JFOM's are concerned, when power is supplied they should become active. As shown in

Figure 3-3, the power management for the JFOM's is arranged by connections between the JPD and two connectors on the EVA panel which also each contain the fiber optic pair. In the JPD, the outputs of a pair of DC-DC converters are dioded together to provide a single power source for the JFOMs. From the JPD these lines are routed to both of the EVA connectors. One of these connectors contains three 16AWG jumpers. From the EVA connectors two sets of power lines return and are connected either back to the JPD and thence to the backplane or directly to the backplane. The jumpers assure that in flight only one JFOM is active. The total cable length between the JPD, EVA panel and either back to the JPD and then to the J-Crate or directly to the J-Crate may approach 10m and excessive voltage drop must be avoided.

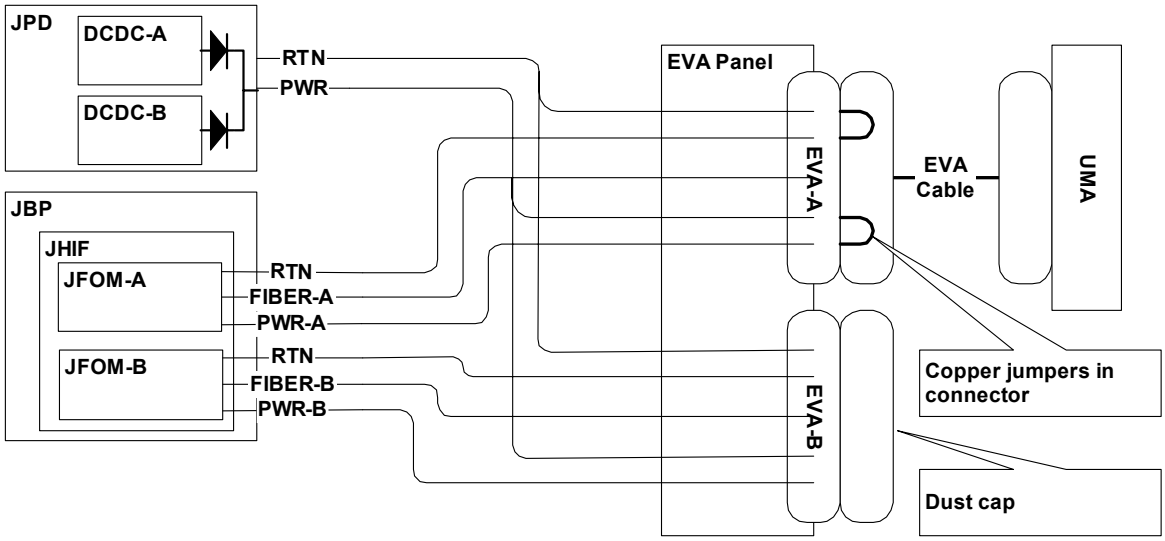


Figure 3-3 - JHIF Power Management

3.2 JLIF

The JLIF is a CompactPCI form factor board, but with no connection to the four cPCI buses. Its function is to provide an interface between the JIM-1553 boards found in each of the four MDCs and the two EVA connectors for 1553 provided on the EVA panel.

3.2.1 The ISS 1553 Interface

Figure 3-4 shows the 1553 cabling for ISS operations.

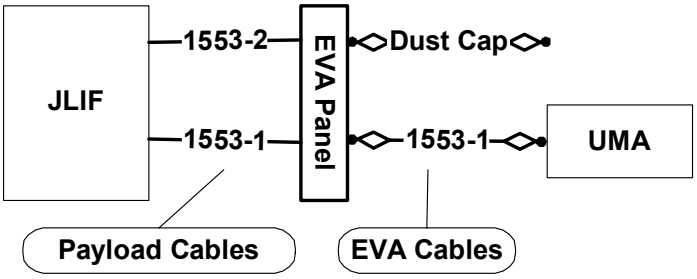


Figure 3-4 – 1553 Integration

The JLIF board is attached by "Payload Cables" to the "EVA Panel". This panel serves to mount connectors that can be exchanged by the flight crew during a space walk.

The Umbilical Mechanism Assembly (UMA) is the connector to the ISS avionics. When the AMS-02 is berthed to ISS the UMA connecter is mated providing connections for the 1553 bus and address lines (and also power and HRDL).

3.2.2 JLIF Implementation Details

The primary purpose of the JLIF is to provide the fan-out/logical-or function for the 1553 serial data streams. The proposed functional diagram for the JIM-1553 and J1553M module is presented in Figure 3-5. The JLIF board would have two J1553M modules for redundancy.

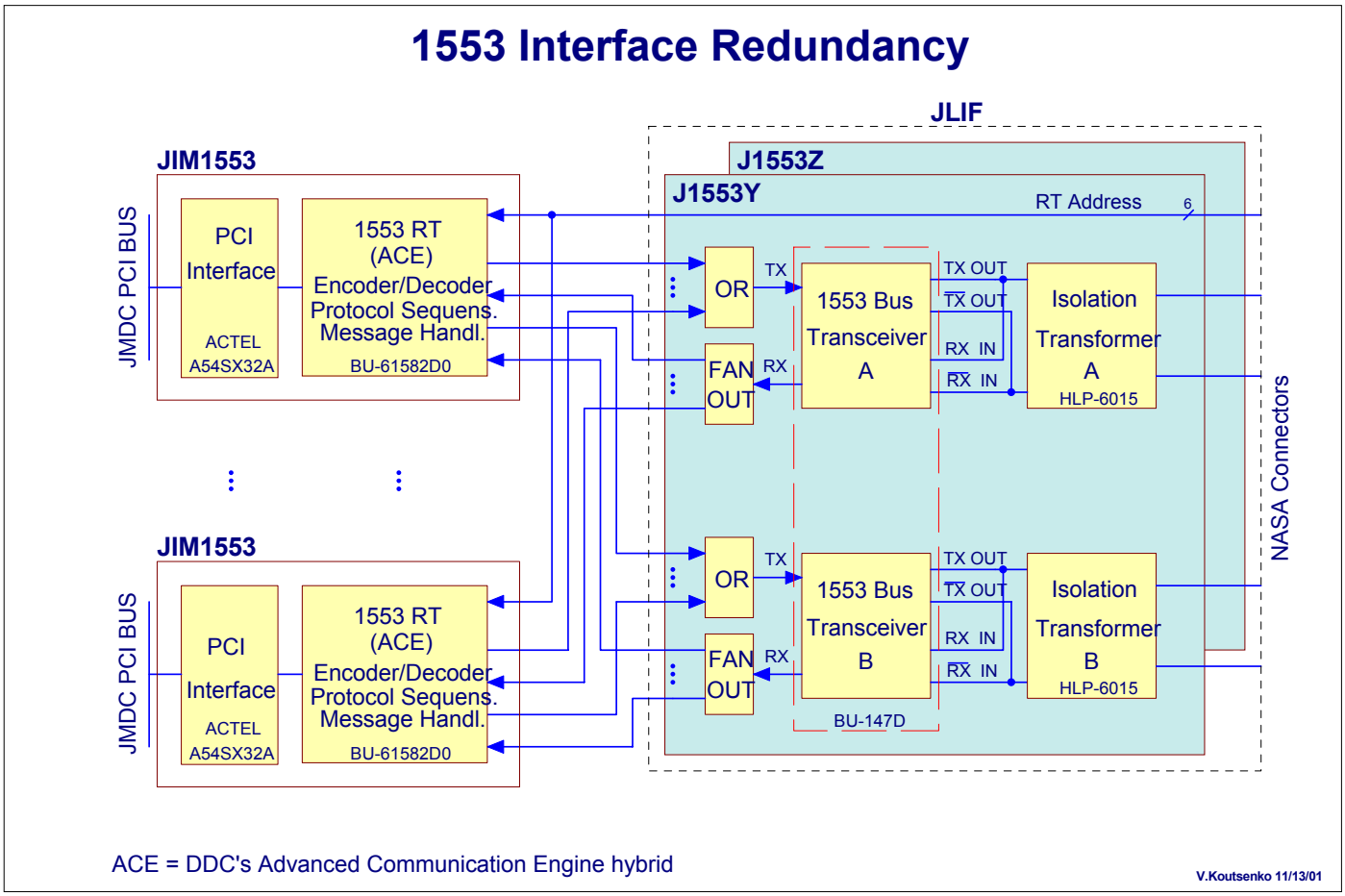


Figure 3-5 - JIM-1553 and JLIF

3.2.3 1553 Address Detection

The operation of the 1553 interface on ISS requires setting a remote terminal (RT) address based on six jumper wires provided by the ISS. The JLIF board must provide an interface to these signals and distribute them out to the four JIM-1553 boards.

The following diagram shows the implementation of the address jumpers for the ISS UMA connector. The address shows jumpers installed for bits 0, 1, 2 and no connects for bits 3, 4 and the parity bit.

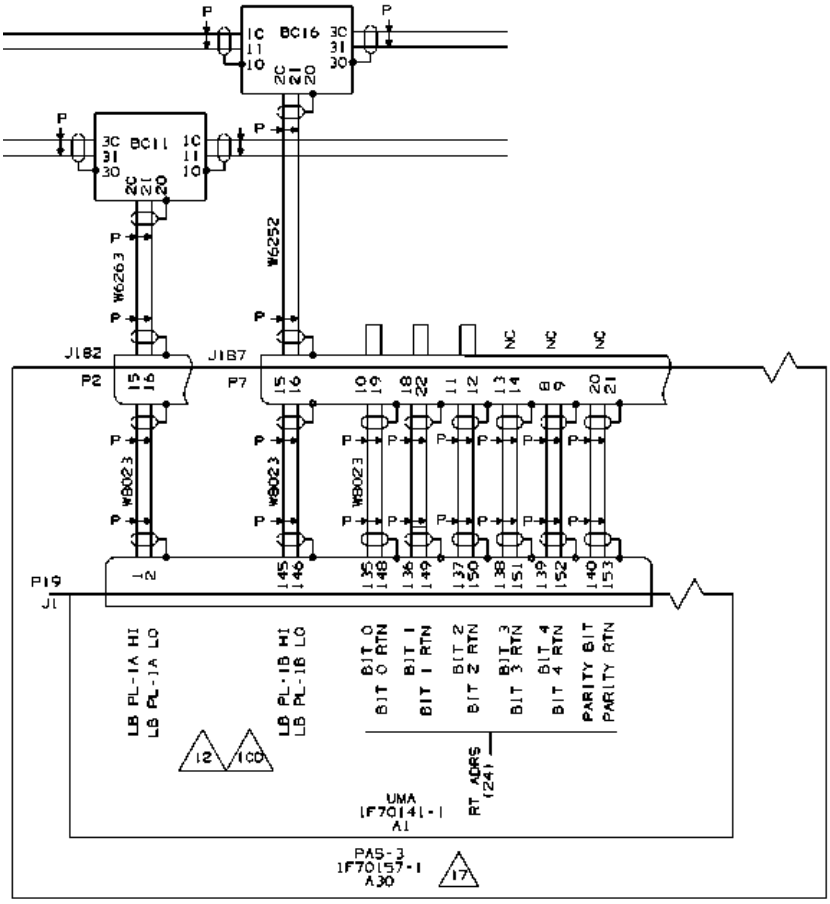


Figure 3-6 – 1553 Address Straps on ISS

Wiring for these signals is 22AWG twisted pair and the length should not exceed 7 meters.

Each JLIF module will have circuitry to power these connections and sense which shunts are present. This circuitry will include parity detection and a logic level signal indicating correct parity. When the parity is correct this circuitry drives the 1553 address on to a set of JBP signals for reception by the JIM-1553 boards.

The EVA connector at the UMA does not have connections to the STS_DECTECTION pair present, resulting in an open circuit.

3.2.4 Power Management on the JLIF Board

A simple jumper within the back shell of the EVA connector selects power to one of the two modules on the JLIF board.

4 STS 1553 Connections

4.1 The STS 1553 Interface

The Remotely Operated Electrical Umbilical (ROEU) is the connecter that attaches to

AMS-02 while it is in the Shuttle. The ROEU comes as a kit with a cable harness and the ROEU Panel serves as a transition point for this harness to the AMS wiring.

The Standard Mixed Cargo Harness (SMCH, pronounced “smitch”) is the NASA standard wiring harness from the payload bay into the flight deck. The Payload Data Interface Panel (PDIP) is a panel mounted in the aft flight deck area providing crew access to connecters and switches associated with a payload.

When AMS is removed from the STS payload bay the ROEU is de-mated, breaking all connections to the PDIP

4.2 STS 1553 RT Address

The 1553 RT address to be used during Shuttle operations is set by configuration of jumper-resistors during the assembly of the JIM_AMSW-1553 board.

5 Integration to STS and ISS

The following diagrams provide the views of AMS when it is attached to the Space Shuttle and ISS and indicates the relationship to the respective avionics systems. They are offered with little explanation and, of course, are out of date.

TBP 1 - Dennett – Get updates into CDR

NOTES: (Both diagrams)

- 1553 Address bits are not in ROEU they are on JIM-1553 board in MDC.
- Show 1553 fan out
- Move 1553 to MDC
- Remove Bus Monitor from STS

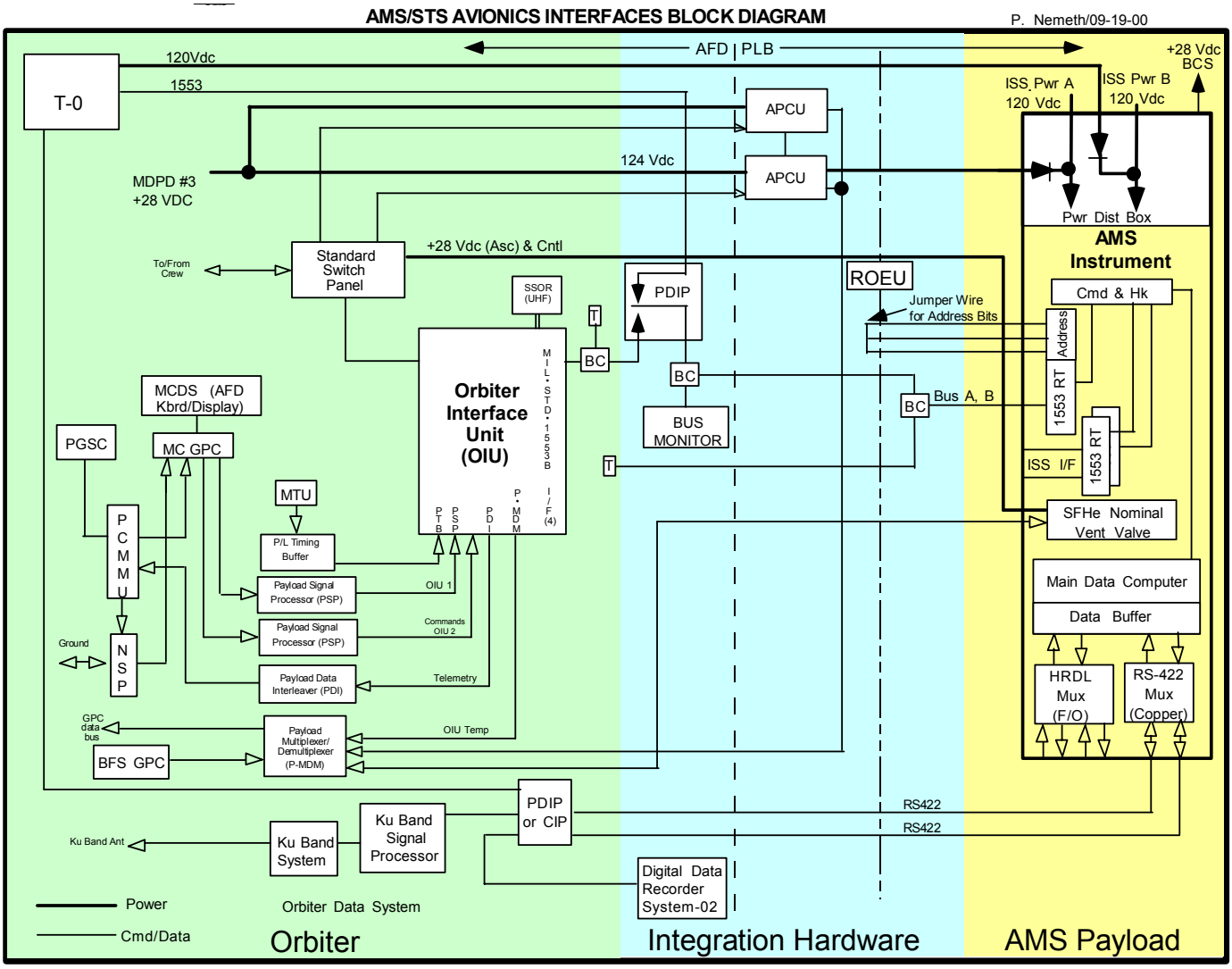


Figure 5-1 - AMS/STS Avionics Interfaces

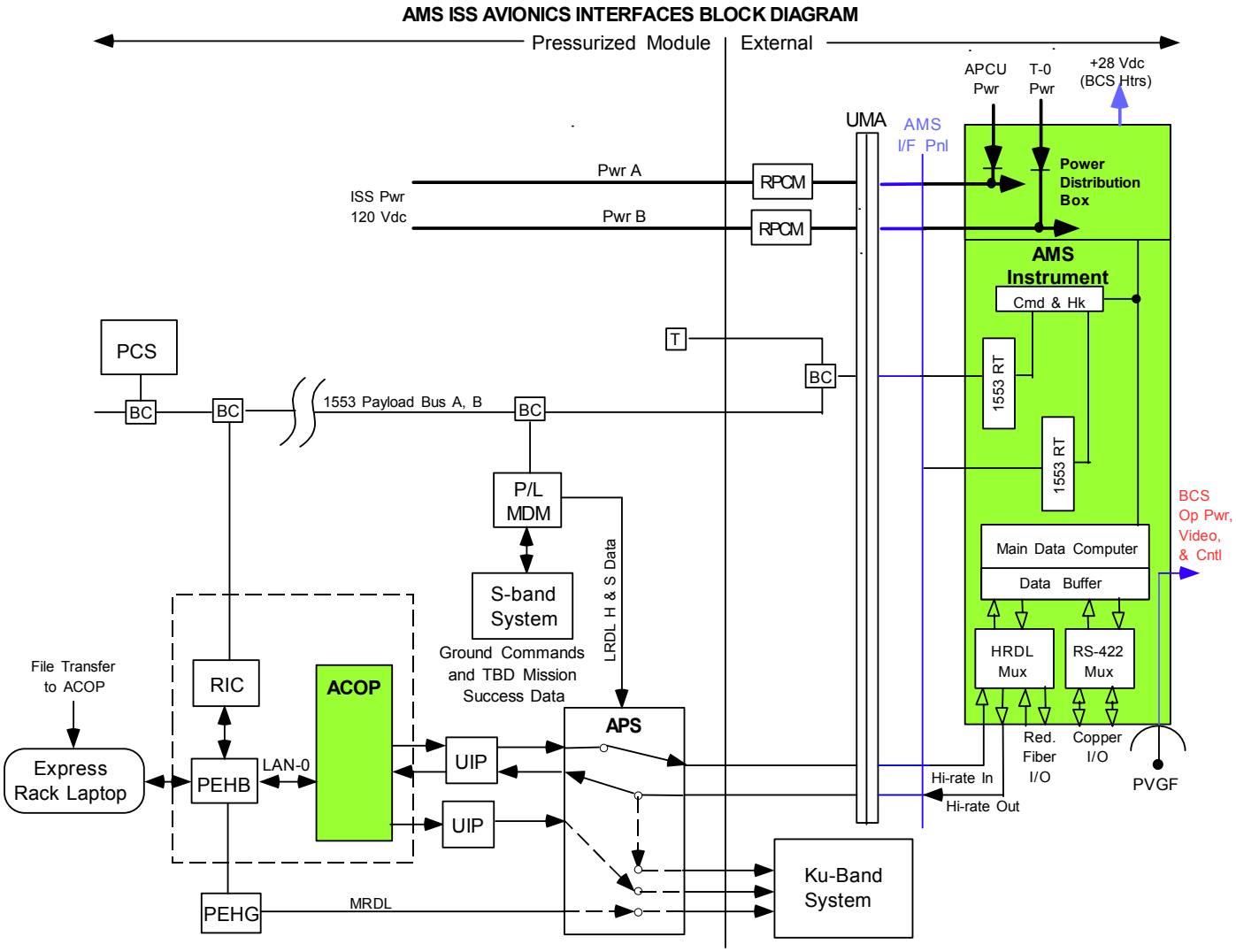


Figure 5-2 – ISS Integration Diagram

AMS-02 System I/F Diag

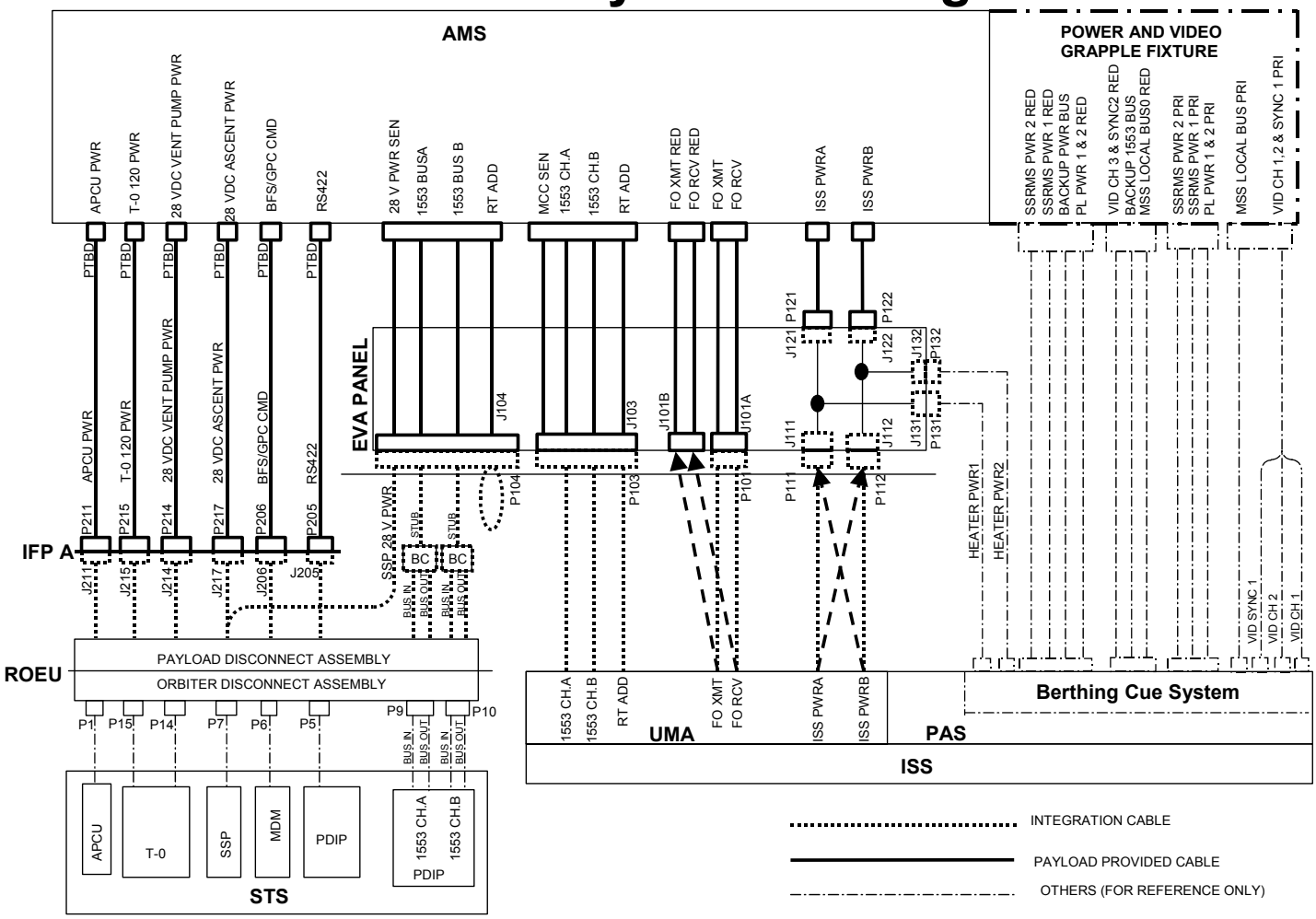


Figure 5-3 - System Interface Diagram

6 J-Crate Overall Specifications

- Power input to JPD is 28 volts, conditioned to lower voltages as required and delivered to J-Crate.
- Power consumption to be minimized.
- Mass to be minimized.
- Storage temperature –40^{o} to 100^{o} C
- Operating temperature, at the crate wall, of –30 to +55 C
- CompactPCI backplanes with 22 slots coordinated into one JBP.
- Redundancy of top-level DAQ system is implemented via four JMDCs.
- STS and ISS flight compatible (extended temp, vibration, out-gassing)
- Conductive Cooling to AMS Crate design

7 Functional Description

7.1 J-Crate Power Up Sequence

The JPD is powered from the PDB by a 28-volt feed. On initial application of 120-volts to the PDB feed the PDB by default provides 28-volts to the J-Crate feed. This 28-volt feeds power the crate heaters under thermostat control. The JPD DC-DC converters for the JMDCs are disabled by thermostat when out of limits.

When the JPD first receives power on its 28-volt feed (and is within temperature limits) power is enabled to all JMDCs. All JMDCs hence power on and:

1. The MDC Power Monitor Circuits on each MDC asserts the JPB_COLD_START signal and sets the POWER_ON_DETECT flip-flop (see below).
2. The hardware reset to each JIM-1553 clears any Remote Terminal (RT) mode. Later it will be placed in Bus Monitor (BM) mode.
3. Each MDC performs cold and warm start sequences (see below)
4. Each MDC enters the boot PROM code where the POWER_ON_DETECT flip-flop is read. Later in the startup software POWER_ON_DETECT is reset by the CPU.
5. If the POWER_ON_DETECT flip-flop is set this is an indication to the boot ROM software that the system should await an external command prior to proceeding with execution of the startup software.

A particular MDC will be commanded to activate its 1553 as an RT. The remaining MDCs will remain in BM mode.

A particular MDC will be commanded to become the unique HRDL or RS422 interface.

In the case that the command source to enable the 1553 is the 1553 itself all JIM-1553s will be in BM mode and there will not be a valid 1553 response to this command. The ISS PLMDM attempts 1553 transmissions three times (with 100ms delays) prior to reporting an error. Best efforts in this particular case should be given to enable an RT within this time frame to reduce error reports.

The system may pow**e**r down (at any stage) selected JMDCs by sending commands on the CAN bus to the USCM controlling the JPD.

7.2 JMDC Power Up and Reset Sequences

The JPD provides ±5.0 and +3.3 voltage to JBP connectors independently for each MDC. These voltages are sequenced on operationally.

The powering of the JHIF and JLIF is discussed in sections 3.1.5 and 3.2.5.

7.2.1 Power Monitoring

The JSBC board will provide a power monitor circuit for both the 3.3v and 5.0v supplies of the MDC. The 3.3v power monitor circuit will hold an MDC in reset until the power is stable.

The 5.0v power monitor reset signal should be latched when activated and the latched results will be provided as input to the CPU for software reading. The software shall have the means to request this latch be cleared. If the 5.0v reset is still asserted this request is ignored and the latch continues to report the current 5.0v power monitor reset state.

The purpose of this is to provide a means for the software to determine both the current operational condition of the 5.0v devices as well as any discontinuity.

7.2.2 POWER_ON_DETECT Flip-flop

This flip-flop is used to provide a means for AMS-02 to have a rapid default automatic recovery path from most upset conditions, while still providing a means to recover from corrupt software or configurations.

The following is a summary of the requirements for the POWER_ON_DETECT flip-flop:

1. Only the 3.3v power monitor's detection of stable power sets this flip-flop.
2. This setting must be complete prior to the CPU entering run state.
3. No other system reset activity (i.e.: #PBRST, WDT, …) has an effect on POWER_ON_DETECT.
4. The CPU reads POWER_ON_DETECT.
5. Only the CPU, via software, resets POWER_ON_DETECT.

7.2.3 JMDC Cold Start Sequence

When power is first applied to a JMDC the Power Monitor Circuits on each JSBC asserts the JPB_COLD_START signal. It is key to note that only the JSBC power monitor circuit's actions determines a cold start.

7.2.4 JMDC Reset and Warm Start Sequence

The JMDC system is reset whenever the hardware reset, as controlled by the assertion of the RST# signal from the PCI bus, is asserted. This signal can be asserted by at least the following scenarios:

- Cold start, as detected by the JSBC power monitor
- Watch dog timer expiration by the JSBC
- Boot command detected by: JIM-AMSW, JIM-HRDL, JIM-RS422, JIM-1553, or JIM-CAN which asserts JPD_PRST (pushbutton reset) causing JSBC to

assert RST#

When the RST# reset signal is asserted it is distributed to all system components via the PCI bus, this includes the CPU and north bridge. The assertion of the reset signal instigates on all system components an initialization of their internal and external interfaces to a consistent state in preparation of the system entering the nominal run state.

The AMS-02 initialization is a bit more selective then for a commercial system. In particular:

- The JBU contents should be preserved.
- The contents of JIM dual port rams are preserved since they may contain boot commands containing parameters.

A warm start sequence is entered anytime the system transitions out of reset. During the reset the CPU and north-bridge are conditioned to begin execution of the code contained at the start of the boot PROM. The warm start sequence is completed when the boot PROM execution is started.

7.2.5 JMDC Boot PROM Start Sequence

When the CPU detects de-assertion of the reset signal, it enters the run state and begins execution of the boot PROM code.

It is the responsibility of the boot PROM code to complete initialization of the system and decide upon its future operation. This includes:

- Initialize and checkout the hardware.
- Determine the source of the reset signal.
- If a cold start instigated this reset enter a command process loop awaiting direction.
- If a boot command instigated this reset: obtain the boot parameters within the appropriate JIM module and generate a reply to the boot command. Based on boot command parameters:
  - Load program from FLASH and execute it.
  - Load program from boot source and execute it.
  - Load program from boot source and write to FLASH, then execute it.
- If no boot command is found (and not cold start), load the “default” program from FLASH and execute it.

During any boot and or reset the Boot PROM code always conditions JIM-1553 for bus monitor mode, the HRDL or RS422 (need to work details around these interfaces) for input, and the CAN interface for input/output.

When JPB_COLD_START is asserted the boot PROM code in the MDC remains in control and monitors for commands addressed to this MDC from each of the above interfaces. While in this mode the MDC boot ROM code has the ability to: enable 1553 RT support, route commands from it's interfaces (1553, RS422, and HRDL) to the CAN bus, write FLASH files via file transfer, and (FBI). When commanded to do so the Boot PROM code clears the JPB_COLD_START signal and proceeds to execute the requested (or default) application program.

The warm start sequence ends when the boot PROM code begins execution of the requested program.

7.3 J-Crate Addressing

The JBP provides each MDC with shunts defining an MDC address. The JIM boards to identify their MDC as the target of a boot command use these address bits. Implementation details are provided within the JBP design document.

7.4 Boot Command Handling by JIM Boards

7.4.1 General Handling for Boot Blocks

The JIM_HRDL, JIM_422, JIM-AMSW, JIM-1553, and JIM_CAN boards each must be able to detect receipt of a boot block and instigate a warm start (as defined above) of the JMDC. When a boot block is detected, and the entire frame containing the block has been received, the JIM board activates the JPD_PRST signal (pushbutton reset) by pulling the signal low for 100 milliseconds.

7.4.2 JIM-422 Boot Block Pattern

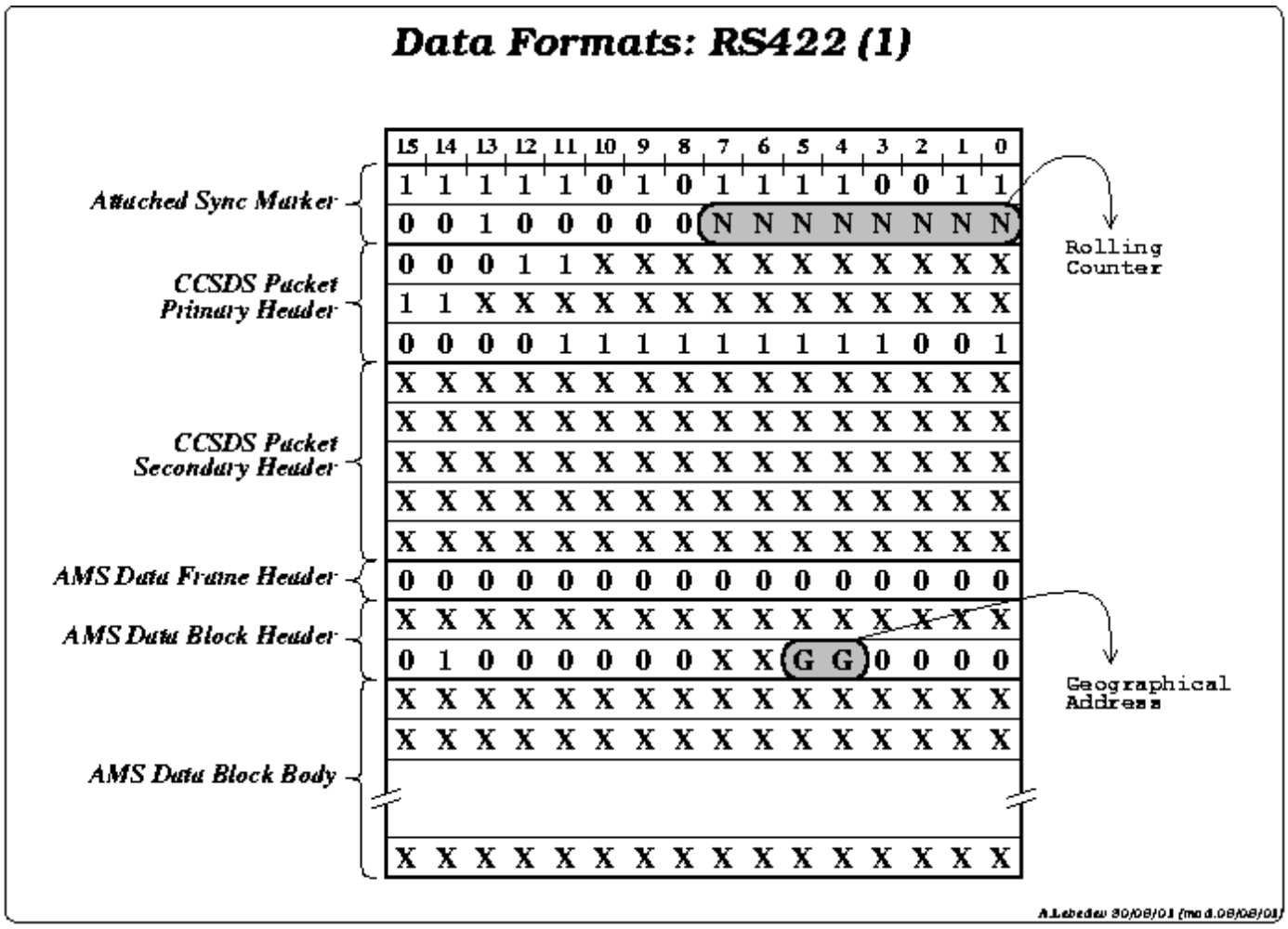


Figure 7-1 – RS422 Boot Command Pattern

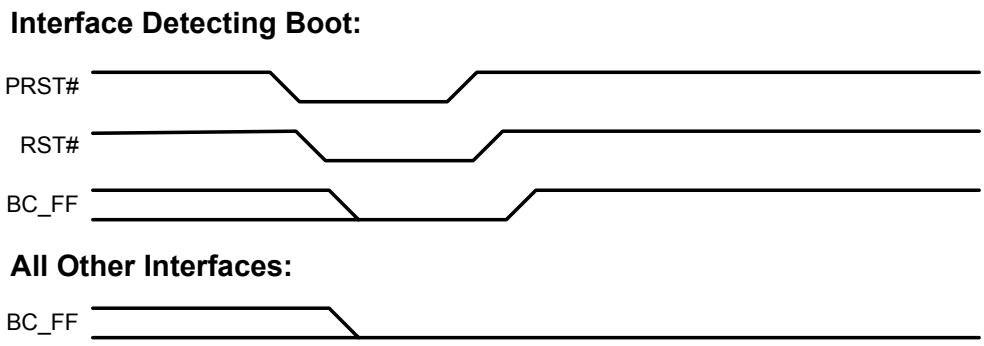
Figure 7-1 defines the pattern for a transmission frame that is a boot block as used on

the RS422. GG is the JMDC ID.

7.4.3 Other Boot Block Patterns

Details for the design of other boot blocks are forth coming. These blocks will be very similar to the RS422 one above.

7.4.4 JIM Board Handling of PRST During Boot Command



BC_FF: Boot Command Flip Flop (Reported as bit in some register to software).

1. RST# Raising edge clears all BC_FFs in system.
2. Interface detecting boot command sets BC_FF on falling edge of RST#.
3. Each interface has its own BC_FF (JIM_AMSW has 3 such bits).
4. The interface(s) to receive boot command has BC_FF set (on "tie" boot using the first one found).
5. Software has no means to clear or set BC_FF.

Figure 7-2 PRST Handling During Boot Command

Note: The interface detecting the boot command should assert the BC_FF signal no later then 1ms after the RST# is de-asserted.

8 JBP

This section provides specifications for the JBP signals and power specific to the AMS backplane implementation. It should be noted that where possible the CompactPCI backplane standard is followed for both signals and power. The intent being that boards built for AMS-02 be interchangeable with standard commercial boards and that standard commercial boards should function within the AMS-02 system subject to limitations of power and function. There is not a requirement for a generic system but where possible the system should be as standard as possible.

8.1 Summary of JBP Signals

The following system logic signals (does not include AMS-Wire, HRDL, 422, or 1553 serial signals) are required on the backplane:

Name	Description	Topology	Domain	Source
JBP_STS	Asserted during operations on the Shuttle	Bus	JBP	JLIF
JBP_1553AD0..5	1553 Address bits	Bus	JBP	JLIF
JBP_COLDSTART	MDC is cold starting	Bus	MDC	JSBC
JBP_PRST#	Push button reset from each JIM slot	Bus	MDC	JIMs
JBP_GA0..1	MDC Geographical id	Bus	MDC	JBP

[a] Point to Point

Figure 8-1 - Summary of JBP Signals

9 Verification Requirements

These requirements are used to define manufacturing tests.

9.1 JIM_HRDL and JHIF

Testing for the HRDL optical system is based on the: "Abstract Test Suite for FDDI Physical Medium Dependent Conformance Testing ANSI X3.225-1996" as well as locally and ISS program developed test methodologies.

9.1.1 Transmitter Optical Power

Measured directly by an optical power meter. The signal being transmitted is to be at 50% duty cycle and shall be:

Min	Max
-10.8dBm	-7.9dBm

9.1.2 Transmitter Optical Characteristics

Parameter	Value	Notes
Nominal Pulse Duration	8 ns	
Signaling Rate	125 MBaud +/- 0.1%	Signaling rate independent of data rate. As specified in ISO/IEC 9314-1:1988 para. 5.2.7.
Signal Extinction Ratio	5% maximum	Tailored requirement; consistent with MDA Transmitter Hybrid specification.
Waveform Rise Time	3.0 ns maximum (1)	Tailored requirement

Waveform Fall Time	3.0 ns maximum (1)	Tailored requirement
Total Jitter	2.36 ns peak-peak maximum	Sum of duty cycle distortion, data dependent jitter, and random jitter, as specified in ISO/IEC 9314-3:1990 Table 1
Duty Cycle Distortion	1.0 ns maximum	Tailored requirement
Data Dependent Jitter		Not measured. (TBR)
Random Jitter		Not measured. (TBR)
(1) The transmitter waveform rise and fall times are more constraining than the waveform figure. The HRDL transmit station must comply with both the waveform and the more constraining rise/fall times.		

9.1.3 Receiver Optical Sensitivity

Two values are measured. The optical receiver threshold and a frame error rate at a defined minimum input power.

The frame error rate is measured by software while receiving a stream of CCSDS packets. A CCSDS frame error is determined by checking the validity of the CCSDS header and the CCSDS packet check word.

The receiver threshold test is performed by attenuating the power of the optical input signal downward until the frame error rate is more than 1% and less then 90% of transmitted packets.

The optical receiver threshold shall be not less the -30dBm (TBR).

The frame error rate at –27dBm (TBR) shall be more then .01% (TBR).

10 Performance Requirements

This purpose of this section is to provide information about performance that is required. Note that when sustained rates are given they should include all system and software overhead required to perform the task. This includes CPU, memory, and PCI-bus loading.

10.1 JSBC Performance Information

The following MDC benchmark figures for data transfer rates have been provided by Andrei Kounine.

To maximize internal throughputs of internal PLB and PCI buses for burst mode transfers L1 Data Cache must be enabled and PCI bus must be run in synchronous mode. Corresponding memory regions in SDRAM and PCI memory should be

declared pre-fetchable. In addition, to avoid significant performance penalties L1 Instruction Cache should must be enabled.

The measured throughput rates with these settings are the following: 82 MByte/sec and 50 MByte/sec for PCI burst WRITE and READ transfers, respectively. Single bit operations result in about 4 times lower transfer rates compared with burst transfers. Other useful figures are 118 (116) MByte/sec for write (read) burst transfers between System Memory and PPC internal registers; and 448 (442) MByte/sec for write (read) operations between L1 Cache and PPC internal registers. These figures can be compared with the throughput of AMSWire link of 10 MByte/sec.

10.2 PCI Bus Transfer Rate

Where possible multiple bytes data operations should be employed to optimize PCI bus operation.

10.3 HRDL Transfer Rate

The physical signaling rate for HRDL is fixed at 125 Mbaud. The logical data transfer rate will be much lower. We require at least 20 Mbaud sustained rates from the HRDL system and are hopeful to reach 40 Mbaud sustained rates.

10.4 CAN Bus Transfer Rate

The CAN Bus system is expected to be capable of sustaining a 1 Mbaud transfer rate from the JSBC to a CAN Bus target (including all overhead of moving data from the JSBC to JIM-CAN).

10.5 RS422 Transfer Rate

The RS422 transfer physical signal rate is fixed at 1.96 Mbaud for transmission and will not exceed 1.96 Mbaud for reception. The system is expected to be able to sustain these rates indefinitely.

11 Mechanical and Thermal Interfaces

This section provides primarily links to web documents with mechanical details. An index of the current applicable documents can be found at:

http://ams.cern.ch/AMS/Electronics/Mech/

11.1 cPCI Board Assembly Drawing

Drawings of the cPCI board assembly, including details for the stiffener and card-guides can be found at:

http://ams.cern.ch/AMS/Electronics/Mech/cPCI_board_assy.pdf

Drawings of the cPCI board mechanical layout can be found at:

http://ams.cern.ch/AMS/Electronics/Mech/cPCI_PCB_layout.pdf

11.2 Thermal Interfaces

The thermal interface, at the board level, is provided by card-guides. The product selected is the *Calmark Corporation Series 260 "card-lok" retainer (cold plate).* The Data sheet for this product can be found at:

http://ams.cern.ch/AMS/Electronics/Mech/series260.pdf

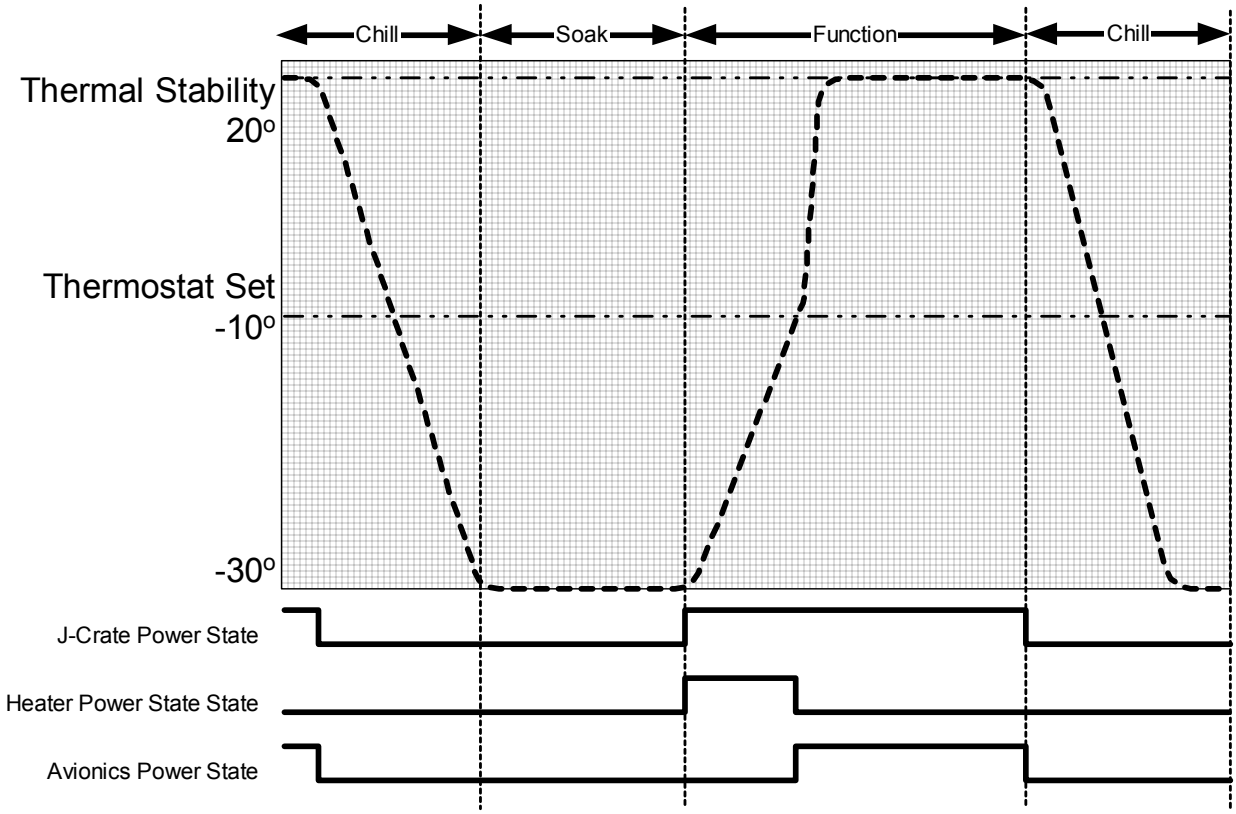


Figure 11-1 - Cold State Operations Profile

12 APPENDIX

12.1 Related Documents

- "AMS-2 DAQ SYSTEM JSBC Prototype BOARD HARDWARE DESIGN SPECIFICATION"; Document No. :CSIST-AMS-MDC-001-R02; CSIST Electronics Systems Division
- "AMS-2 DAQ SYSTEM JBU Prototype BOARD HARDWARE DESIGN SPECIFICATION"
- "AMS-2 DAQ SYSTEM JIM-AMSWIRE PROTOTYPE BOARD HARDWARE DESIGN SPECIFICATION"; Document No. :CSIST-AMS-MDC-002-R02; CSIST Electronics Systems Division
- "DAQ JHRDL/USRT HARDWARE DESIGN SPECIFICATION FOR ALPHA MAGNETIC SPECTROMETER (Draft)"
- "DAQ HRDL FUNCTIONAL DESCRIPTION FOR ALPHA MAGNETIC SPECTROMETER (Draft)"
- "AMS-2 DAQ SYSTEM JIM-USRT Prototype BOARD HARDWARE DESIGN SPECIFICATION"; Document No. ???; CSIST Electronics Systems Division
- "AMS-2 DAQ SYSTEM JIM-CAN Prototype BOARD HARDWARE DESIGN SPECIFICATION"; Document No. ???; CSIST Electronics Systems Division
- "AMS-02 DAQ JFOM Prototype Board Hardware Design Specification

GLOSSARY

422	See RS422
1553	MIL Standard, high reliability serial communications link
6U	A Euro standard PCB form factor
ACC	Anti coincidence counter. A detector
ACOP	AMS Crew Operations Post. A data recorder with command abilities used on ISS
ACOPjr	A laptop based system used on STS
AMS	Alpha Magnetic Spectrometer
AMS-02	The new design AMS system will be put on space station at duration about 3 year
AMS-wire	A serial point to point communication protocol, also AMSWire and just AMSW
ASIC	Application specific integrated circuit
A/D	Analog to digital
BC	Bus Coupler. A interface device to a 1553 bus
BM	Bus Monitor. A mode of operation for a 1553 device
CAN	Controller Area Network. A serial communication bus
CDDC	Command distributor and data concentrator module, located on the on the JINF (two each) and JINJ (one) boards.
CDP	Common digital Part. A FPGA and DSP based common hardware for detector front ends
cPCI	Compact PCI
Ecal	Electronic Calorimeter. A detector
EVA	Extra Vehicular Activity (Space Walk)
EVA Panel	A panel mounting the EVA connectors
EVA Connector	Space qualified connector suitable for handling by an astronaut while space walking
Event	A unit of science data on AMS. Typically about 2000 bytes of data recording the information about passage of a particle through the detectors.
FLASH	Re-programmable non-volatile memory
FPGA	Field programmable gate array
Front End	The electronics interfacing detectors and the DAQ system
DAQ	Data acquisition (system)
DDRS	Digital data recording system

HRDL	High rate data link. Fiber optic data link on ISS
ISS	International space station
J422	RS422 Multiplex module
JBP	J-Crate Backplane
JBU	JMDC Memory buffer board
JFOM	Fiber optic Multiplex module
JHIF	J-Crate high rate interface board
JIM	JMDC Interface module board
JLIF	J-Crate low rate interface board
JMDC	Main DAQ computer (AKA MDC)
JPD	J-Crate Power Distributor
JSBC	JMDC Single board computer
KU	Space to ground communications system (KU-band)
Latch-up	A heavy ion cosmic ray radiation induced failure of a circuit some times resulting in excessive power consumption and circuit destruction
LRDL	Low rate data link. A 1553 serial data connection
MDC	Main DAQ computer (AKA JMDC)
OIU	Orbiter Interface Unit. The bus master of 1553 on STS
Orbiter	Space shuttle
PCI	Peripheral Component Interconnect
PCI Agent	FPGA based cPCI interface to local peripherals
PDB	Power Distribution Box. The fuse box of AMS-02
PDIP	Payload Data Interface Panel. A panel on the aft flight deck of STS
PICMG	PCI Industrial Computer Manufacturers Group
PLMDM	Payload Multiplexer/De-multiplexer. Serves as the 1553 bus master. Provides routing for commands to payloads and reads telemetry (health and status) for downlink.
PROM	Programmable Read Only Memory. Commonly infers one time programming
ROEU	Remotely Operated Electronics Umbilical. Connector between AMS-02 and STS
ROM	Read Only Memory. Most often means PROM
RS422	In fact an electrical standard specifying signaling on a single twisted pair. Used in the context here to specify a serial data stream protocol carried over several RS422 twisted pairs.
RT	Remote Terminal. A mode of operation for a 1553 device
SDRAM	Synchronous DRAM

STS	Space Transportation System (Space Shuttle)
TBD	To be defined
TBM	To be modified
TBR	To be reviewed
ToF	Time of Flight. A detector
Tracker	A silicon based particle detector
Trigger	Electronics associated with detecting passage of a particle based on detector activity. Also used to describe software based filtering of observed events
UMA	Umbilical Mechanism Assembly. Connector between AMS-02 and ISS
USCM	Universal slow control module. A micro controller based module attached to the CAN bus
xDR2	A class of Data Reduction boards for front ends with two CDPs on board